

REMARKS

This Preliminary Amendment responds to the Office Action dated March 23, 2005 in which the Examiner rejected claims 1-5 under 35 U.S.C. §102(b), stated that claims 8-12 are allowed and objected to claim 6 as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

As indicated above, claim 6 has been rewritten into independent form.

Therefore, Applicants respectfully requests the Examiner withdraws the objection thereto.

As indicated above, claim 1 has been amended to incorporate claim 3. The amendment is unrelated to a statutory requirement for patentability.

Claim 1 claims a modulator using a delta-sigma conversion method, and comprises component separating unit, single-stage delta-sigma modulator and output operating unit. The component separating unit separates a signal component and an error component of a digital input signal from each other. The single-stage delta-sigma modulator modulates the error component separated by the component separating unit. The output operating unit operates the signal component separated by the component separating unit and the error component modulated by the single-stage delta-sigma modulator. The single-stage delta-sigma modulator includes a plurality of integrators, a quantizer and a delay element. The quantizer quantizes an output of the integrator in a final stage. The delay element delays an output of the quantizer to perform negative feedback by sending the delayed output to the plurality of integrators.

Through the structure of the claimed invention including a modulator with a plurality of integrators, a quantizer quantizing a final stage of the integrators and a

delay element delaying the output of the quantizer to perform negative feedback to the plurality of integrators as claimed in claim 1, the claimed invention provides a modulator which can improve stability and precision. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claims 1-5 were rejected under 35 U.S.C. §102(b) as being anticipated by *Karema et al.* (U.S. Patent No. 5,061,928).

Karema et al. appears to disclose a method of cascading two or more sigma-delta modulators by applying an error signal representing the quantization error of a preceding modulator to a subsequent modulator in the cascade to be quantized therein, the quantized error signal being thereafter differentiated and subtracted from the quantized output signal of the preceding modulator. (col. 1, lines 9-14) The system of FIG. 1 comprises two substantially identical second-order sigma-delta modulators A and B. Each modulator A and B comprises a series-connection of the following components in this order: a summing means 1, an integrating means 2 (or filter), a summing means 7, an integrating means 4 (or filter) and a quantization unit or comparator 6 at the output of which a final quantized signal D1 or D2 occurs. Each modulator A and B comprises a two-part negative feedback. The feedback comprises a switching unit 10 having an input to which the quantized output signal D1 or D2 is applied and an output connected through a scaling means 8 to one input in the summing means 1 to be subtracted from the input signal and through a scaling means 9 to one input in the summing means 7 to be subtracted from the output signal of the first integrator 2. The switching unit 10 connects either a positive reference voltage +REF or a negative reference voltage -REF to its output, depending on the state of the quantized output signal D1 and D2. The first scaling

means 8 scales the output of the switching unit 10 with the number 1 while the second scaling means 9 scales the output of the switching unit 10 with the number 2. The blocks 3 and 5 in FIG. 1 illustrate the delay contained in the integrating means 2 and 4, respectively. Since both integrators 2 and 4 comprise a delay in this specific case, the transfer function of the modulators A and B will be equal to one when the ratio of the scaling factor of the first scaling means 8 to that of the second scaling means 9 is 1:12. (col. 3, lines 37-68)

Thus, *Karema et al.* merely discloses modulators A, B comprising a summing means, an integrating means 2, a summing means 7, an integrating means 4, a quantization unit 6, a switching unit 10, a scaling means 8, 9 as well as delay elements 3, 5. Thus, *Karema et al.* has a structure different from claim 1 and in particular nothing in *Karema et al.* shows, teaches or suggests a modulator including a plurality of integrators, a quantizer quantizing an output of the integrator in a final stage and a delay element delaying an output of the quantizer to perform negative feedback by sending the delayed output to the plurality of integrators as claimed in claim 1. Rather, *Karema et al.* teaches away from the claimed invention since the delay elements are inserted between the integrators 2 and summing element 7 or integrators 4 and quantizer 6.

Since nothing in *Karema et al.* shows, teaches or suggests the structure of the modulator as claimed in claim 1, Applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(b).

Claims 2 and 4-5 depend from claim 1 and recite additional features. Applicants respectfully submit that claims 2 and 4-5 would not have been anticipated by *Karema et al.* within the meaning of 35 U.S.C. §102(b) at least for the reasons as

set forth above. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 2 and 4-5 under 35 U.S.C. §102(b).

Since claim 3 has been incorporated into claim 1, Applicants respectfully submit that there are no new issues for consideration.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge
our Deposit Account No. 02-4800.

Respectfully submitted,

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